

CLAIMS

1. An access circuit structure for selectively providing an externally accessible terminal with access to each of a plurality of circuit wells fabricated in a semiconductor substrate and isolated from each other, the access circuit structure comprising for each of the circuit wells:

a first transistor fabricated in a well formed in the semiconductor substrate that is isolated from the circuit wells, the first transistor having a first source-drain region fabricated in the well and being coupled to the externally accessible terminal and to the well, a second source-drain region fabricated in the well, and a gate electrode fabricated between the first and second source-drain regions of the first transistor and coupled to receive a first select signal for the respective circuit well, the first transistor being fabricated in the well in a manner that causes a first diode to be formed between the source and drain regions of the first transistor; and

a second transistor fabricated in a well formed in the semiconductor substrate that is isolated from the circuit wells, the second transistor having a first source-drain region fabricated in the well and being coupled to the second source-drain region of the first transistor, a second source-drain region fabricated in the well and being coupled to the well and to a respective one of the circuit wells, and a gate electrode fabricated between the first and second source-drain regions of the second transistor and coupled to receive a second select signal for the respective circuit well, the second transistor being fabricated in the well in a manner that causes a second diode to be formed between the source and drain regions of the second transistor, the second diode being coupled to the first diode in a back-to-back configuration.

2. The access circuit structure of claim 1 wherein the first select signal and the second select signal comprise a common select signal.

3. The access circuit structure of claim 1 wherein the well in which the first transistor is fabricated is different from the well in which the second transistor is fabricated.

4. The access circuit structure of claim 3 wherein the substrate comprises an n-type substrate, and the wells in which the first and second transistors are fabricated and the circuit wells comprise respective p-type wells.

5. An access circuit for selectively providing an externally accessible terminal with access to each of a plurality of circuit wells fabricated in a semiconductor substrate and isolated from each other, each of the circuit wells having a respective semiconductor circuit fabricated therein, the access circuit comprising for each of the circuit wells:

a first transistor fabricated in a well formed in the semiconductor substrate that is isolated from the circuit wells, the first transistor having a first source-drain region fabricated in the well and being coupled to the externally accessible terminal and to the well, a second source-drain region fabricated in the well, and a gate electrode fabricated between the first and second source-drain regions of the first transistor and coupled to receive a first select signal for the respective circuit well, the first transistor being fabricated in the well in a manner that causes a first diode to be formed between the source and drain regions of the first transistor;

a second transistor fabricated in a well formed in the semiconductor substrate that is isolated from the circuit wells, the second transistor having a first source-drain region fabricated in the well and being coupled to the second source-drain region of the first transistor, a second source-drain region fabricated in the well and being coupled to the well and to a respective one of the circuit wells, and a gate electrode fabricated between the first and second source-drain regions of the second transistor and coupled to receive a second select signal for the respective circuit well, the second transistor being fabricated in the well in a manner that causes a second diode to be formed between the source and drain regions of

the second transistor, the second diode being coupled to the first diode in a back-to-back configuration;

a first control circuit for applying the first select signal to the gate electrode of the first transistor responsive to a first access signal, the control circuit comprising:

a shunt transistor having a gate terminal and a pair of source-drain terminals coupled between the externally accessible terminal and the gate electrode of the first transistor; and

a control transistor having a gate terminal coupled to receive the first access signal, the control transistor having a pair of source-drain terminals coupled between the externally accessible terminal and the gate terminal of the shunt transistor; and

a second control circuit for applying the second select signal to the gate electrode of the second transistor responsive to a second access signal.

6. The access circuit of claim 5 wherein the semiconductor circuit fabricated in each of the circuit wells comprises a memory circuit.

7. The access circuit of claim 6 wherein each of the memory circuits comprises a respective dynamic random access memory circuit.

8. The access circuit of claim 6 wherein each of the memory circuits comprises an array of memory cells.

9. The access circuit of claim 8 wherein each of the arrays of memory cells comprises an array of dynamic random access memory cells.

10. The access circuit of claim 5 wherein the second control circuit is identical to the first control circuit.

11. The access circuit of claim 5 wherein the first control circuit further comprises a first switching transistor having a gate terminal coupled to receive the access signal, and a pair of source-drain terminals coupled between a supply voltage and the gate terminal of the control transistor.

12. The access circuit of claim 11 wherein the first control circuit further comprises a second switching transistor having a gate terminal coupled to receive a compliment of the access signal, and a pair of source-drain terminals coupled between the supply voltage and the gate terminal of the shunt transistor.

13. The access circuit structure of claim 5 wherein the well in which the first transistor is fabricated is different from the well in which the second transistor is fabricated.

14. The access circuit of claim 13 wherein the substrate comprises a p-type substrate, and the wells in which the first and second transistors are fabricated and the circuit wells comprise respective n-type wells.

15. The access circuit of claim 5 wherein the second control circuit comprises:

a shunt transistor having a gate terminal and a pair of source-drain terminals coupled between the externally accessible terminal and the gate electrode of the second transistor; and

a control transistor having a gate terminal coupled to receive the second access signal, the control transistor having a pair of source-drain terminals coupled between the externally accessible terminal and the gate terminal of the shunt transistor.

16. The access circuit of claim 5 wherein the first access signal and the second access signal comprise a common access signal.

17. In a memory device having a plurality of memory array cores each including a memory array fabricated in a respective memory core well formed in a semiconductor substrate and isolated from each other, a plurality of access circuits each of which selectively couples an externally accessible terminal to a respective one of the memory core wells, each of the access circuits comprising:

a first transistor fabricated in a well formed in the semiconductor substrate that is isolated from the memory core wells, the first transistor having a first source-drain region fabricated in the well and being coupled to the externally accessible terminal and to the well, a second source-drain region fabricated in the well, and a gate electrode fabricated between the first and second source-drain regions of the first transistor and coupled to receive a first select signal for the respective circuit well, the first transistor being fabricated in the well in a manner that causes a first diode to be formed between the source and drain regions of the first transistor;

a second transistor fabricated in a well formed in the semiconductor substrate that is isolated from the circuit wells, the second transistor having a first source-drain region fabricated in the well and being coupled to the second source-drain region of the first transistor, a second source-drain region fabricated in the well and being coupled to the well and to a respective one of the circuit wells, and a gate electrode fabricated between the first and second source-drain regions of the second transistor and coupled to receive a second select signal for the respective circuit well, the second transistor being fabricated in the well in a manner that causes a second diode to be formed between the source and drain regions of the second transistor, the second diode being coupled to the first diode in a back-to-back configuration;

a first control circuit for applying the first select signal to the gate electrode of the first transistor responsive to a first access signal; and

a second control circuit for applying the second select signal to the gate electrode of the second transistor responsive to a second access signal.

18. The access circuit of claim 17 wherein each of the first and second control circuits comprise:

a shunt transistor having a gate terminal and a pair of source-drain terminals coupled between the externally accessible terminal and the gate electrode of a respective one of the first and second transistors; and

a control transistor having a gate terminal coupled to receive a respective one of the first and second access signals, the control transistor having a pair of source-drain terminals coupled between the externally accessible terminal and the gate terminal of the shunt transistor.

19. The access circuit of claim 18 wherein each of the control circuits comprise a first switching transistor having a gate terminal coupled to receive the respective access signal, and a pair of source-drain terminals coupled between a supply voltage and the gate terminal of the control transistor.

20. The access circuit of claim 19, further comprising a second switching transistor having a gate terminal coupled to receive a compliment of the respective access signal, and a pair of source-drain terminals coupled between the supply voltage and the gate terminal of the shunt transistor.

21. The access circuit structure of claim 17 wherein the well in which the first transistor is fabricated is different from the well in which the second transistor is fabricated.

22. The access circuit of claim 21 wherein the substrate comprises a p-type substrate, and the wells in which the first and second transistors are fabricated and the memory core wells comprise respective n-type wells.

23. A control circuit for applying a select signal to a gate electrode of a pass transistor responsive to an access signal, the transistor having gate-source terminals coupled between first and second terminals, the control circuit comprising:

a shunt transistor having a gate terminal and a pair of source-drain terminals coupled between the first terminal and the gate electrode of the pass transistor; and

a control transistor having a gate terminal coupled to receive the access signal, the control transistor having a pair of source-drain terminals coupled between the first terminal and the gate terminal of the shunt transistor.

24. The control circuit of claim 23, further comprising a first switching transistor having a gate terminal coupled to receive the access signal, and a pair of source-drain terminals coupled between a supply voltage and the gate terminal of the control transistor.

25. The control circuit of claim 24, further comprising a second switching transistor having a gate terminal coupled to receive a compliment of the access signal, and a pair of source-drain terminals coupled between the supply voltage and the gate terminal of the shunt transistor.

26. A memory device, comprising:

a row address circuit operable to receive and decode row address signals applied to external address terminals of the memory device;

a column address circuit operable to receive and decode column address signals applied to the external address terminals;

a plurality of memory cell arrays each operable to store data written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals, each of the memory cell arrays being fabricated in a respective array well formed in a semiconductor substrate and isolated from each other;

a data path circuit operable to couple data signals corresponding to the data between each of the arrays and external data terminals of the memory device;

a command decoder operable to decode a plurality of command signals applied to respective external command terminals of the memory device, the command decoder being operable to generate control signals corresponding to the decoded command signals;

a plurality of access circuits each of which selectively couples a predetermined one of the external terminals to a respective one of the array wells, each of the access circuits comprising:

a first transistor fabricated in a well formed in the semiconductor substrate that is isolated from the array wells, the first transistor having a first source-drain region fabricated in the well and being coupled to the predetermined external terminal and to the well, a second source-drain region fabricated in the well, and a gate electrode fabricated between the first and second source-drain regions of the first transistor and coupled to receive a first select signal for the respective array well, the first transistor being fabricated in the well in a manner that causes a first diode to be formed between the source and drain regions of the first transistor;

a second transistor fabricated in a well formed in the semiconductor substrate that is isolated from the array wells, the second transistor having a first source-drain region fabricated in the well and being coupled to the second source-drain region of the first transistor, a second source-drain region fabricated in the well and being coupled to the well and to a respective one of the array wells, and a gate electrode fabricated between the first and second source-drain regions of the second transistor and coupled to receive a second select signal for the respective array well, the second transistor being fabricated in the well in a manner that causes a second diode to be formed between the source and drain regions of the second transistor, the second diode being coupled to the first diode in a back-to-back configuration;

a first control circuit for applying the first select signal to the gate electrode of the first transistor responsive to a first access signal; and

a second control circuit for applying the second select signal to the gate electrode of the second transistor responsive to a second access signal.

27. The memory device of claim 26 wherein each of the first and second control circuits comprise:

a shunt transistor having a gate terminal and a pair of source-drain terminals coupled between the predetermined external terminal and the gate electrode of a respective one of the first and second transistors; and

a control transistor having a gate terminal coupled to receive a respective one of the first and second access signals, the control transistor having a pair of source-drain terminals coupled between the predetermined external terminal and the gate terminal of the shunt transistor.

28. The memory device of claim 27 wherein each of the control circuits comprise a first switching transistor having a gate terminal coupled to receive the respective access signal, and a pair of source-drain terminals coupled between a supply voltage and the gate terminal of the control transistor.

29. The memory device of claim 28, further comprising a second switching transistor having a gate terminal coupled to receive a compliment of the respective access signal, and a pair of source-drain terminals coupled between the supply voltage and the gate terminal of the shunt transistor.

30. The memory device of claim 26 wherein the well in which the first transistor is fabricated is different from the well in which the second transistor is fabricated.

31. The memory device of claim 30 wherein the semiconductor substrate comprises an n-type substrate, and the wells in which the first and second transistors are fabricated and the array wells comprise respective p-type wells.

32. The memory device of claim 26 wherein each of the memory cell arrays fabricated in a respective one of the array wells comprise a dynamic random access memory cell array.

33. The memory device of claim 26 wherein the second control circuit is identical to the first control circuit.

34. A computer system, comprising:
a processor having a processor bus;
an input device coupled to the processor through the processor bus to allow data to be entered into the computer system;
an output device coupled to the processor through the processor bus to allow data to be output from the computer system;
a data storage device coupled to the processor through the processor bus to allow data to be read from a mass storage device;
a memory controller coupled to the processor through the processor bus; and
a memory device coupled to the memory controller, the memory device comprising:
a row address circuit operable to receive and decode row address signals applied to external address terminals of the memory device;
a column address circuit operable to receive and decode column address signals applied to the external address terminals;
a plurality of memory cell arrays each operable to store data written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals, each of the memory cell arrays being fabricated in a respective array well formed in a semiconductor substrate and isolated from each other;
a data path circuit operable to couple data signals corresponding to the data between each of the arrays and external data terminals of the memory device;
a command decoder operable to decode a plurality of command signals applied to respective external command terminals of the memory device, the command decoder being operable to generate control signals corresponding to the decoded command signals;

a plurality of access circuits each of which selectively couples a predetermined one of the external terminals to a respective one of the array wells, each of the access circuits comprising:

a first transistor fabricated in a well formed in the semiconductor substrate that is isolated from the array wells, the first transistor having a first source-drain region fabricated in the well and being coupled to the predetermined external terminal and to the well, a second source-drain region fabricated in the well, and a gate electrode fabricated between the first and second source-drain regions of the first transistor and coupled to receive a first select signal for the respective array well, the first transistor being fabricated in the well in a manner that causes a first diode to be formed between the source and drain regions of the first transistor;

a second transistor fabricated in a well formed in the semiconductor substrate that is isolated from the array wells, the second transistor having a first source-drain region fabricated in the well and being coupled to the second source-drain region of the first transistor, a second source-drain region fabricated in the well and being coupled to the well and to a respective one of the array wells, and a gate electrode fabricated between the first and second source-drain regions of the second transistor and coupled to receive a second select signal for the respective array well, the second transistor being fabricated in the well in a manner that causes a second diode to be formed between the source and drain regions of the second transistor, the second diode being coupled to the first diode in a back-to-back configuration;

a first control circuit for applying the first select signal to the gate electrode of the first transistor responsive to a first access signal; and

a second control circuit for applying the second select signal to the gate electrode of the second transistor responsive to a second access signal.

35. The computer system of claim 34 wherein each of the first and second control circuits comprise:

a shunt transistor having a gate terminal and a pair of source-drain terminals coupled between the predetermined external terminal and the gate electrode of a respective one of the first and second transistors; and

a control transistor having a gate terminal coupled to receive a respective one of the first and second access signals, the control transistor having a pair of source-drain terminals coupled between the predetermined external terminal and the gate terminal of the shunt transistor.

36. The computer system of claim 35 wherein each of the control circuits comprise a first switching transistor having a gate terminal coupled to receive the respective access signal, and a pair of source-drain terminals coupled between a supply voltage and the gate terminal of the control transistor.

37. The computer system of claim 36, further comprising a second switching transistor having a gate terminal coupled to receive a compliment of the respective access signal, and a pair of source-drain terminals coupled between the supply voltage and the gate terminal of the shunt transistor.

38. The computer system of claim 34 wherein the well in which the first transistor is fabricated is different from the well in which the second transistor is fabricated.

39. The computer system of claim 38 wherein the semiconductor substrate comprises an n-type substrate, and the first and second wells and the array wells comprise respective p-type wells.

40. The computer system of claim 34 wherein each of the memory arrays fabricated in a respective one of the array wells comprise a dynamic random access memory array.

41. The computer system of claim 34 wherein the second control circuit is identical to the first control circuit.

42. A method of applying a test voltage to each of a plurality of circuit wells fabricated in a semiconductor substrate of an integrated circuit and isolated from each other, the method comprising:

applying a test voltage to the integrated circuit through an externally accessible terminal; and

coupling the externally accessible terminal to one of the circuit wells while isolating the externally accessible terminal from the other circuit wells regardless of the magnitude and polarity of the test voltage.

43. The method of claim 42 wherein the act of coupling the externally accessible terminal to one of the circuit wells while isolating the externally accessible terminal from the other circuit wells comprises:

providing first and second transistors fabricated in respective wells of the substrate for each of the circuit wells, the first and second transistors having first source-drain regions interconnecting to each other and second source-drain regions coupled to the wells in which they are fabricated;

coupling the first and second transistors for each of the circuit wells between the externally accessible terminal and the respective circuit well;

applying signals to gate electrodes of the first and second transistors for the one circuit well that causes the first and second transistors to turn on; and

applying signals to gate electrodes of the first and second transistors for the other circuit wells that causes the first and second transistors to turn off.